PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	Port & Cable Aggregation ECR
DATE:	April 13, 2018
AFFECTED DOCUMENT:	OCuLink 1.0
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Part I

1. Summary of the Functional Changes

The OCuLink workgroup has received feedback that the information included in the specification regarding cable/ Port aggregation was unclear, particularly with respect to sideband management. Wording in sections relating to cable/ Port aggregation and sideband management has been reworked to be clearer.

2. Benefits as a Result of the Changes

Wording is clearer.Cable installation is easier.

3. Assessment of the Impact

Specfication requirements are easier to understand.

4. Analysis of the Hardware Implications

Systems ultilizing aggregated OCuLink Ports may be implemented with less confusion. Aggregated OCuLink cable assemblies may be built to be more effective in systems with aggregated Ports.

5. Analysis of the Software Implications

None; this change does not affect software.

6. Analysis of the C&I Test Implications

None; this change does not affect testing.

Part II

Detailed Description of the change

Change Section 3.4, page 12 as follows:

3.4 Port and Cable Aggregation

Note: These Ports are aggregated in the same order as Ports specified in the larger *PCI Express External Cable Specification*.

3.4.1. x4 Host and Peripheral Fixed Host Board-side Connector Aggregation

Host and peripheral Ports are permitted to be designed to support Port aggregation. ~~A pair of x4 connectors that supports x8 Port aggregation are permitted t0 operate independently as x4 Ports, or be logically combined to form a single x8 Port. Similarly, a group of four x4 connectors that supports x16 Port aggregation are permitted to operate independently as x4 Ports, or be combined to form a single x16 Port. It is allowable for a pair of connectors to support x8 aggregation and also be part of a group that supports x16 Port aggregation.~~ Connectors that support Port aggregation are permitted to operate as independent x4 Ports or combined to form single, larger Ports (x8 or x16). For example, two x4 Ports may be combined to operate as a single x8 Port or four x4 Ports may be combined to operate as two x8 Ports or one x16 Port. Moveover, a pair of connectors supporting an aggregated x8 Port may be aggregated again to form part of a x16 Port.

- The x8 and x16 cables must provide the requisite number of x4 Free Cable-side connectors at each end. The relative positioning ~~of the individual x4 connectors must be such that they are able to be mated with the device connector pin and orientation arrangements defined in Figure 3-2 and Figure 3-3. The relative positioning and~~ orientation of the ~~connectors~~ Free Cable-side connectors must be constrained ~~enough to make it very difficult for a user to cross plug the connectors and achieve incorrect~~ such that Lane ordering, as depicted by Figure 3-2 and Figure 3-3, is intuitively maintained when mating to the Host.
- When mated, the connector/cable set must not exceed the mechanical envelope defined by the Fixed Host Board-side connectors (see Chapter 9).

3.4.2. x4 Host and Peripheral Fixed Host Board-side Connector Aggregation Positioning Requirements

The basic Lane numbering and pin numbering for ~~the~~ Fixed Host Board-side connectors is shown in Figure 3-1 for reference. OCuLink ~~The x4~~ Ports~~/connectors~~ (x4, x8, and x16)~~, x8 Ports/connectors, and the x16 Ports/connectors~~ must be aggregated as shown in Figure 3-2 and Figure 3-3 ~~for Board-side connectors as well as the~~ and must meet the marking/labeling requirements listed in Section 8.

The minimum distance between Fixed Host Board-side Ports ~~in both X and Y directions~~ is determined by the ~~minimum pitch~~size of the Free-side cable ~~plug~~ assemblies because~~. Some of the reasons for this are~~:

- Application may require a ~~larger~~ different wire gauge, ~~wire~~ which may change the size~~makes the width of the plug wider and/or higher~~ (width and/or height) of the plug.
- Application may require a cable to exit in a particular ~~from~~ direction ~~the side east or west or to exit north or south~~ which ~~would~~ may interfere with another ~~Port~~ connector in close proximity.
- A Host is permitted to ~~present the~~implement connectors oriented uniformly or belly-to-belly~~w~~. Orientation affects connector spacing and the amount of clearance needed to mate/ unmate cables~~ith the connector orientation facing away from each other, or facing towards each other, which would affect finger clearance and spacing~~.

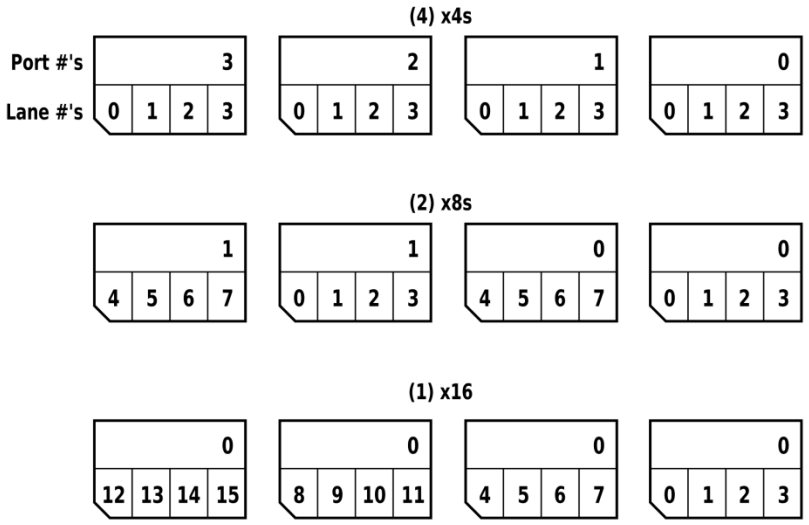

Figure 3-2. Port Aggregation for ~~the~~ x4 Fixed Host Board-side ~~with~~ Connectors with Uniform Orientation ~~Facing the Same Direction~~

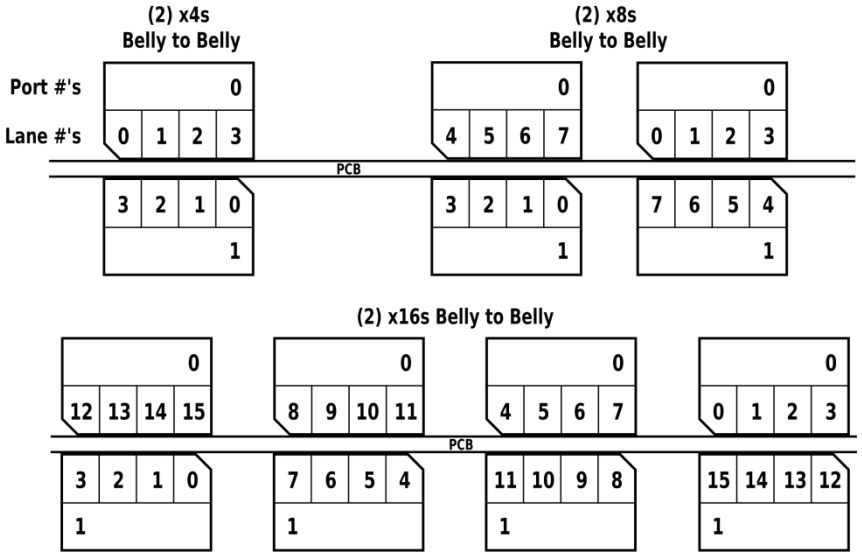

Figure 3-3. Port Aggregation for ~~the~~ x4 Fixed Host Board-side ~~with the~~ Connectors with Belly-to-Belly Orientation ~~Facing Away from Each Other~~

3.4.3. Additional Requirements for Aggregating Cables

- When mated, the connector/cable set must not exceed the mechanical envelope defined by the Fixed and Free connectors in this Specification.
- Cables are ~~also~~ permitted to be aggregated to match specific applications~~,~~ where the host has aggregated Ports~~,~~ or by request from an end user.
- See Chapter 8 for labeling requirements.
- See Appendix F for system level information pertaining to Port aggregation.

Change Appendix A, page 76 as follows:

Appendix A – Cable Management Memory Map

A.2. Upper Page Memory Map

The upper page 00h contains the serial identifiers and is used for read-only identification information. The serial identifier is divided into the base identifier fields (bytes 128 to 191), extended identifier fields (bytes 192 to 223), and vendor-specific data fields (bytes 224 to 255). The format of the Upper Page 00h Memory Map is shown in Table A-1.

EDITOR'S NOTE: Leave other table entries unchanged. Changes shown here superscede changes incorporated via the Memory Map ECN.

Table A-1. Upper Page 00h

Byte	Description	Value	Type	Notes
139	~~Number of Lanes~~Rsvd	~~Bits 2:0~~ ~~001b = 1 Lane~~ ~~010b = 2 Lanes~~ ~~100b = 4 Lanes~~ ~~All others RsvdP~~ ~~Bits 7:3 - RsydP~~	Read Only	~~Value 3 is not a valid entry for this field~~Not used for PCIe; used to indicate number of Lanes in SAS applications
140	~~Supported PCIe rates~~Rsvd	~~Data Rate Identifier~~ ~~Bit 0 – RsvdP~~ ~~Bit 1 – 2.5 GT/s Data Rate~~ ~~Bit 2 – 5.0 GT/s Data Rate~~ ~~Bit 3 – 8.0 GT/s Data Rate~~ ~~Bits 7:4 – RsvdP.~~	Read Only	~~Nominal PCIe Bit Rate; this enables support for Legacy Cables and for future upgrades~~Not used for PCIe; used to indicate supported PCIe rates in SAS applications
141~~-142~~	~~RsvdP~~Free Cable-side connector count	Indicates total number of cables in aggregate assembly	Read Only	Zero if not part of an aggregate cable assembly, legit values are 2+
142	Free Cable-side connector ID	Indicates cable in aggregate assembly	Read Only	Zero if not part of an aggregate cable assembly; legit values are ≤ [Value of Byte 141]
143 - 144	~~Propagation delay~~Rsvd	~~16-bit hex number~~	Read Only	~~Cable propagation delay (one-way), in nanoseconds~~Not used for PCIe; used to indicate propagation delay in SAS applications

Change Appendix F, page 96 as follows:

Appendix F – System Level Port Aggregation

- The Upstream device ~~needs to~~must have Lanes configured into Ports of the desired size and configuration before Link training is able to begin. The method in which this occurs is beyond the scope of this Specification.
- ~~The Upstream Subsystem and Downstream Subsystem must read the cable management Memory Space to determine how each physical cable interface should be configured. However, if the lowest order Cable Port is identified to be a x16, it is permissible to ignore the other Ports.~~
- The method for reading each Port is implementation specific~~.~~:
  - The sideband signals for connector(s) with the lowest order ~~cable Port~~Lane numbers must represent the logical Link ~~and it is permissible to ignore the higher order cable Port sidebands~~.
  - Sideband signals are needed on each cable in an aggregate assembly in order to identify each Free Cable-side connector within the assembly. This is done by reading the memory map from each individual Free Cable-side connector.
- The cable management controller must configure each Port individually, regardless of the logical Port width.